MOS Technology MCS650X microprocessor designers gather around a 200X print of the CPU Rubylith, color-coded for debugging into metallization, polysilicon and diffusion layers. In the background is a 1000X expansion of the internal 21X143 decode-ROM, which manager Chuck Peddle claims is a key factor in obtaining small chip size. From left to right are layout designers Sydney-Anne Holt, Michael Jaynes, Harry Bawcom, design engineers Chuck Peddle, Ray Hirt, Rodney Orgill, William Mensch and Wilbur Mathys. Seated is product manager Terry Holdt. See page 24.

# Does The Country Need A Good $20 Microprocessor?

NORRISTOWN, PA — Is MOS Technology offering a high-performance microprocessor at single-unit prices of $20 just to buy into the CPU business? And, if so, will low profits keep them from providing software and other crucial customer support?

Any answer to these questions based on single-piece prices is probably irrelevant. For one thing, documentation sent out with single-piece orders probably costs more than the CPU itself. For another, only high-volume competition will determine whether the CPU gains a foothold in the marketplace. The company's product manager, Chuck Peddle, claims that, by virtue of high yield on a carefully

planned minimum chip size, he'll compete successfully with enough profit left for reinvestment in ample user support. It isn't going to be easy, though, in view of the recent erosion in volume processor prices. Peddle admits other vendors have already come close to him in high-volume pricing.

"I've deliberately set the single-piece price low enough," says Peddle, "so that anyone looking for TTL replacement in control and measurement systems can't overlook it. We've spoken to over 100 accounts and many of them just won't use, for example, a $40 CPU to interconnect a bunch of PIAs (peripheral interface adapters) they can buy for about $6 each in volume."

As for software, "It pays for itself," says Peddle, "at least at the prices set by my competition. Anyway, as part of the price for getting into the business, we are committed to full software support, as well as to a real-time multi-processor simulating and debugging system.

"The small CPU chip size," Peddle continues, "was a planned effort from the beginning of our design effort.

"We decided on a memory-oriented CPU like the Motorola 6800 rather than one with general-purpose internal registers like the Intel 8080. Internal registers are fine until you run out of registers for a given problem, in which case a lot of extra address coding is required.

"Since the limiting factor in designing to a given chip size is having enough metallization for the instruction data-transfer paths, we talked to potential customers about what instructions they really needed and what could be omitted.

"As a result," Peddle explains, "we left out double–byte stores and reduced the number of machine states from Motorola's 13 to just seven. Then we used a very large ROM rather than hardwired logic for control, which, con-

trary to industry opinion that ROM take too much space, actually reduce the chip size."

While Peddle admits that going t seven states means he can't dump an recall all the CPU contents as quickl as the Motorola 6800 during an inter rupt, he claims it's worth it in reduce chip area. "We tried an eight-stat machine which would dump the ac cumulator as well as the progran counter and status," he says, "bu since it added another 10 mils to th chip, we discarded it."

As for benchmark contests on byt count, Peddle says he's won several o them over equivalent CPUs by 20 pe cent, but doesn't claim he'll win then all. "I'll lose to a user," he admits "with a benchmark that makes op timum use of all the internal register of the 8080."

He does claim a general speed ad vantage per instruction over com petitors, though, with typical clocl rates of 2 MHz. "One reason for th high clock rate," Peddle says, "is tha the large ROM reduced our logical interconnect levels to five and cu overall propagation times."

— *Robert Sugarma*